AMENDMENTS TO THE CLAIMS

1-4. (Cancelled)

5. (New) An extending circuit for memory connected to an external FIFO circuit, said extending circuit for memory being operable to extend a memory capacity used for writing data input to said extending circuit for memory to the external FIFO circuit, said extending circuit for memory comprising:

an internal FIFO circuit;

an output data effective signal generator operable to receive a first status signal output from the external FIFO circuit indicating whether or not the external FIFO circuit can write data therein; and

an internal FIFO write enable generator operable to receive the first status signal output from the external FIFO circuit indicating whether or not the external FIFO circuit can write data therein;

wherein when the first status signal received by said internal FIFO write enable generator indicates that the external FIFO cannot write data therein, said internal FIFO write enable generator is operable to cause said internal FIFO circuit to perform a writing operation of writing the input data into said internal FIFO circuit; and

wherein when the first status signal received by said output data effective signal generator indicates that the external FIFO can write data therein, said output data effective signal generator is operable to output the input data to the external FIFO circuit directly without passing through said internal FIFO circuit, and cause the external FIFO circuit to perform a writing operation of writing the input data into the external FIFO circuit.

6. (New) The extending circuit for memory according to claim 5, wherein said internal FIFO circuit is operable to output a second status signal indicating whether or not said internal FIFO circuit has data written in said internal FIFO circuit.

7. (New) The extending circuit for memory according to claim 6, further comprising:

an internal FIFO read enable generator operable to receive the first status signal output from the external FIFO circuit and the second status signal output from said internal FIFO circuit; and

an output data generator operable to receive the data input to said extending circuit for memory and output data to the external FIFO circuit;

wherein when the first status signal received by said internal FIFO read enable generator indicates that the external FIFO can write data therein and when the second status signal received by said internal FIFO read enable generator indicates that said internal FIFO circuit has data written therein, said internal FIFO read enable generator is operable to cause said internal FIFO circuit to perform a reading operation of reading the data written in said internal FIFO circuit and outputting the read data to the external FIFO circuit; and

wherein when said output data generator receives the data input to said extending circuit for memory, the external FIFO circuit outputs the first status signal indicating that the external FIFO circuit can write data therein and said internal FIFO circuit outputs the second status signal indicating that said internal FIFO circuit has data written therein, said output data generator is operable to output, prior to the received data input to said extending circuit for memory, the data written in said internal FIFO circuit and read out by said internal FIFO circuit to the external FIFO circuit.

8. (New) A transmitting-receiving device using said extending circuit for memory according to claim 7 to be connected with either a transmission FIFO circuit or a reception FIFO circuit in a switching manner in order to extend a memory capacity for either the transmission FIFO circuit or the reception FIFO circuit, said transmitting-receiving device comprising:

a first selector for enabling either a transmission signal system or a reception signal system to be connected with said extending circuit for memory in a switching manner;

a second selector for enabling a third status signal from either the transmission FIFO circuit or the reception FIFO circuit to be received by said internal FIFO write

enable generator, said output data effective signal generator and said internal FIFO read enable generator of said extending circuit for memory in a switching manner;

a third selector for enabling the transmission FIFO circuit to be connected with either said output data generator and said output data effective signal generator of said extending circuit for memory or the transmission signal system in a switching manner; and

a fourth selector for enabling the reception FIFO circuit to be connected with either said output data generator and said output data effective signal generator of said extending circuit for memory or the reception signal system in a switching manner.

9. (New) The transmitting-receiving device using said extending circuit for memory according to claim 8, further comprising a control section for

receiving status signals from the transmission FIFO circuit and the reception FIFO circuit indicating whether or not the transmission FIFO circuit and the reception FIFO circuit can write data therein, respectively,

connecting said first selector with the reception signal system and connecting said second and third selectors with said fourth selector in a switching manner, when the status signal received from the transmission FIFO circuit indicates that the transmission FIFO circuit can write data therein and the status signal received from the reception FIFO circuit indicates that the reception FIFO circuit cannot write data therein, and

connecting said first selector with the transmission signal system and connecting said second and fourth selectors with said third selector in a switching manner, when the status signal received from the transmission FIFO circuit indicates that the transmission FIFO circuit cannot write data therein and the status signal received from the reception FIFO circuit indicates that the reception FIFO circuit can write data therein.